

The diagram illustrates a multi-stage shift register circuit with the following components and connections:

- Stages:** The register consists of several stages, each containing a series of flip-flops or storage elements. The stages are labeled with numbers: 50 (top), 30, 10, 20, 40, and 60 (bottom).
- Control Signals:**
 - DLY-FORWARD:** A control signal line at the top right.
 - VSTOR:** A control signal line on the right side.
 - TCK:** A clock signal line on the right side.
 - DLY-REVERSE:** A control signal line at the bottom right.
- Data Flow and Connections:**
 - A feedback loop is shown on the left, connecting the output of the bottom stage (60) back to the input of the top stage (50).
 - Internal connections within stages are labeled with numbers: 52, 54, 56, 36, 34, 32, 70, 22, 14, 24, 16, 26, 18, 28, 42, 44, 46, 62, 64, 66, and 2'.
 - Arrows indicate the direction of data flow, including a horizontal arrow labeled '2' pointing right and a vertical arrow labeled '2'' pointing down.

FIG. 1

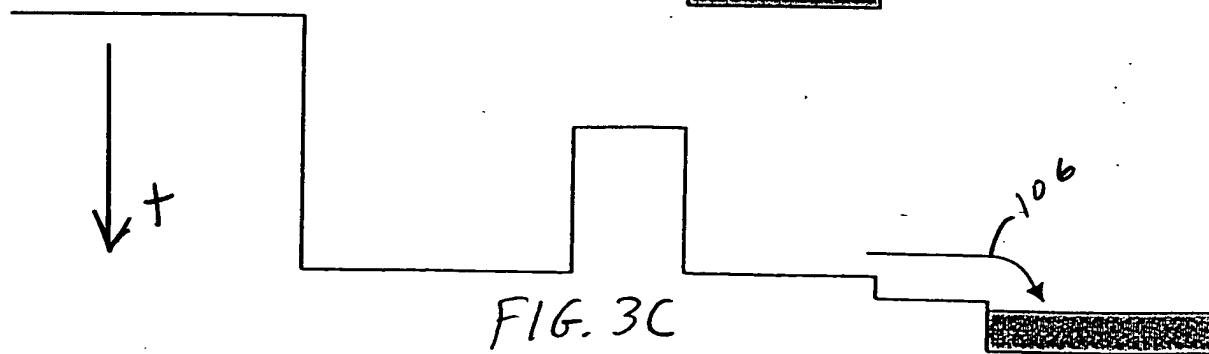
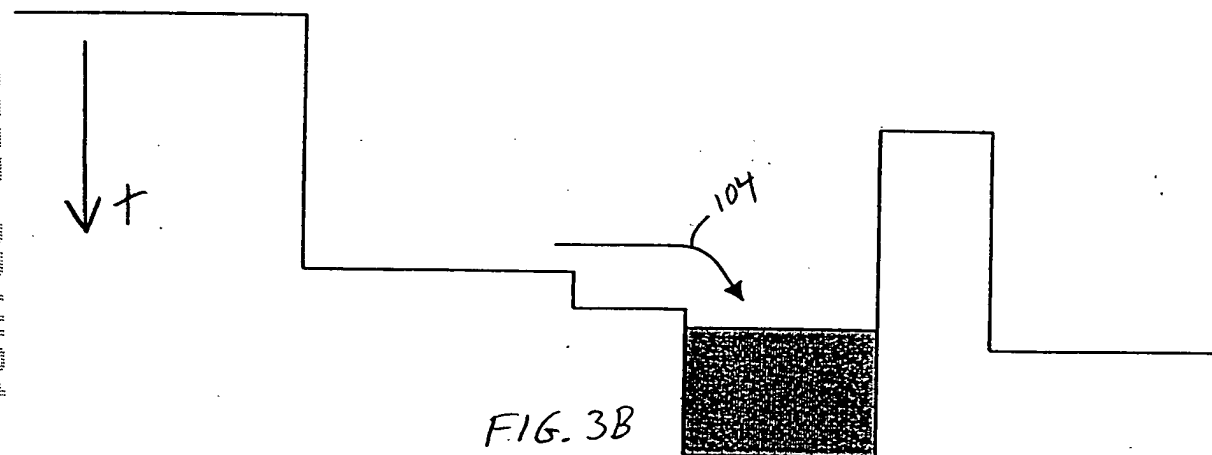
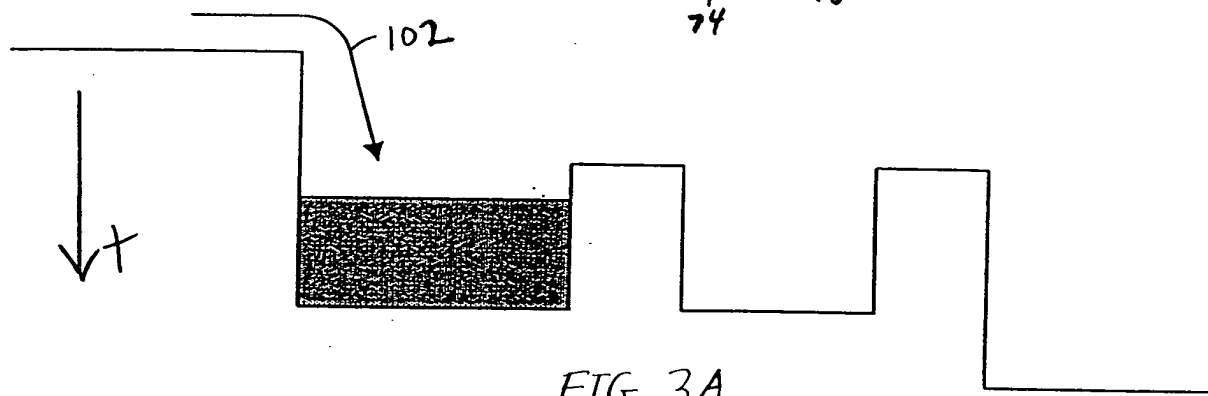
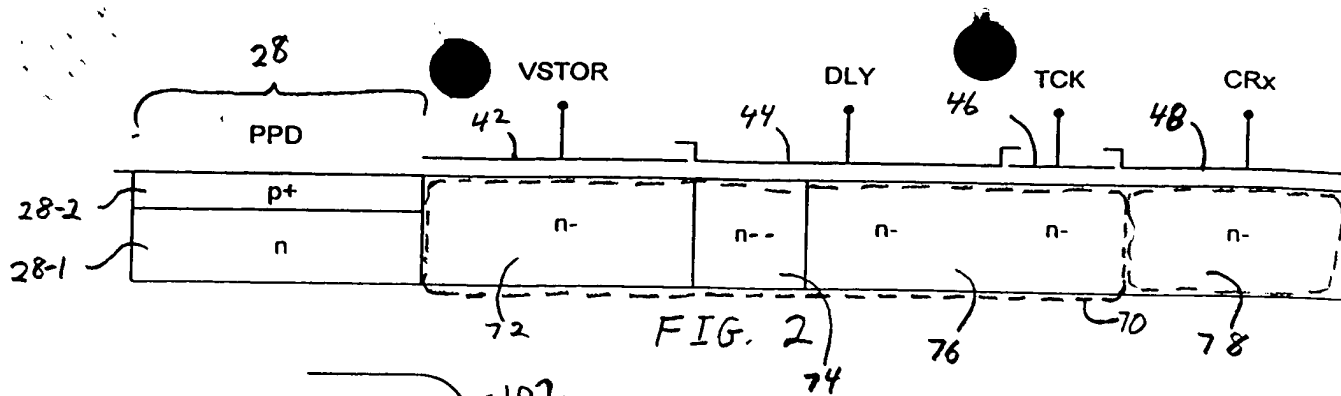


FIG. 2

DLY-FORWARD



TCK



DLY-REVERSE



FIG. 4

DLY-FORWARD



TCK



DLY-REVERSE



FIG. 5

FIG. 4

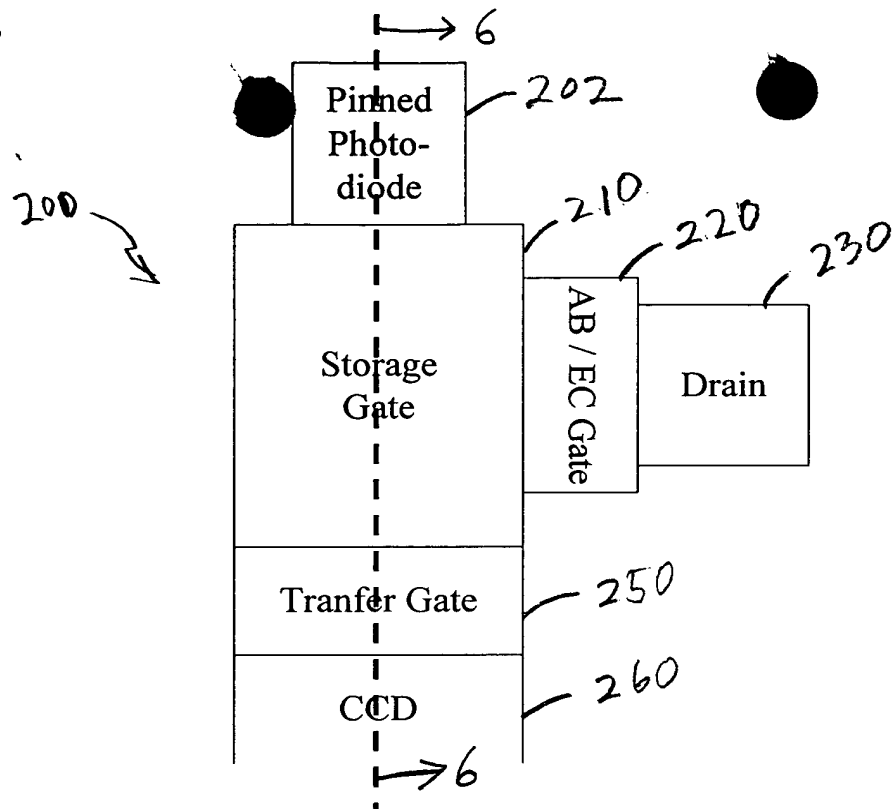


FIG. 6

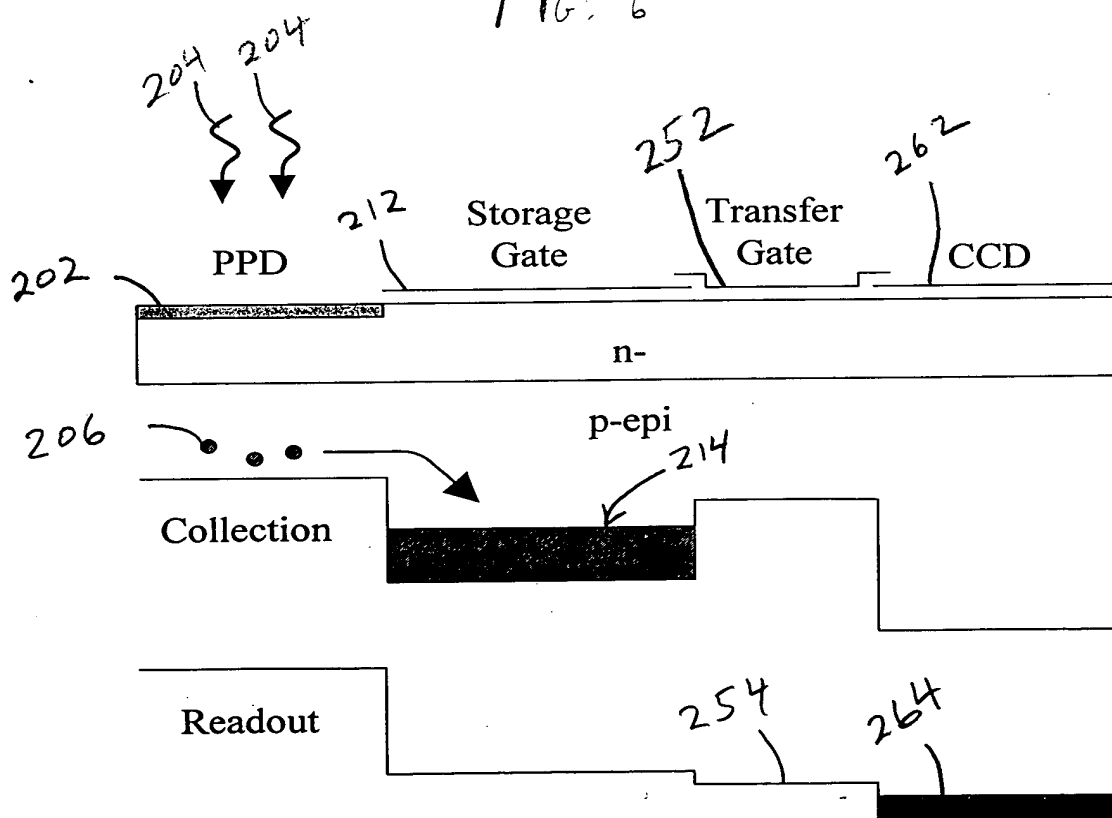


FIG. 7

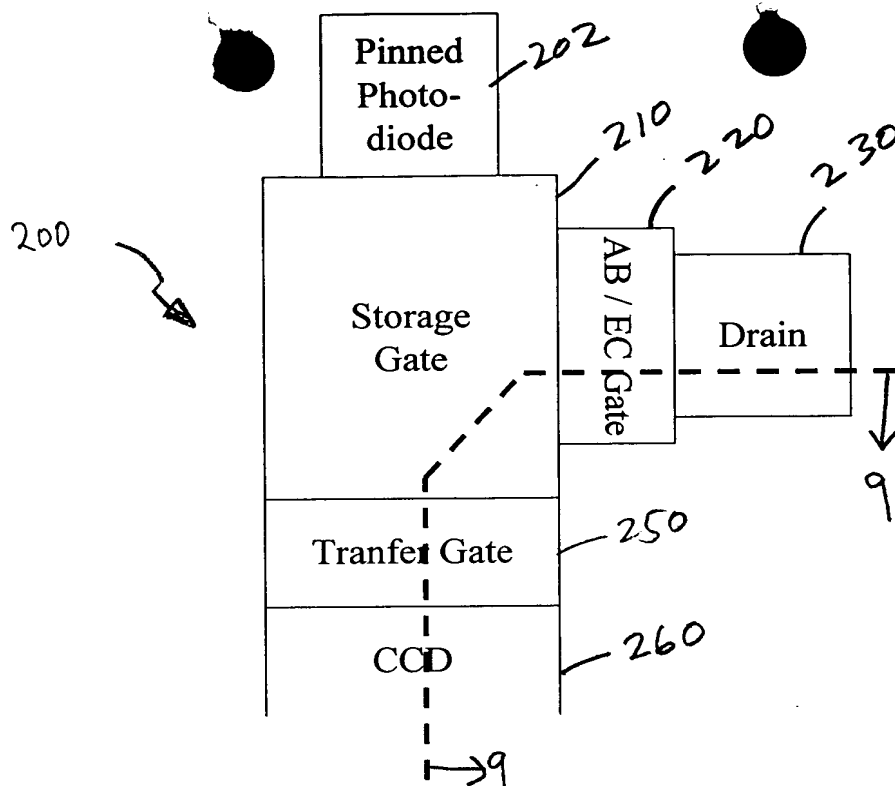


FIG. 8

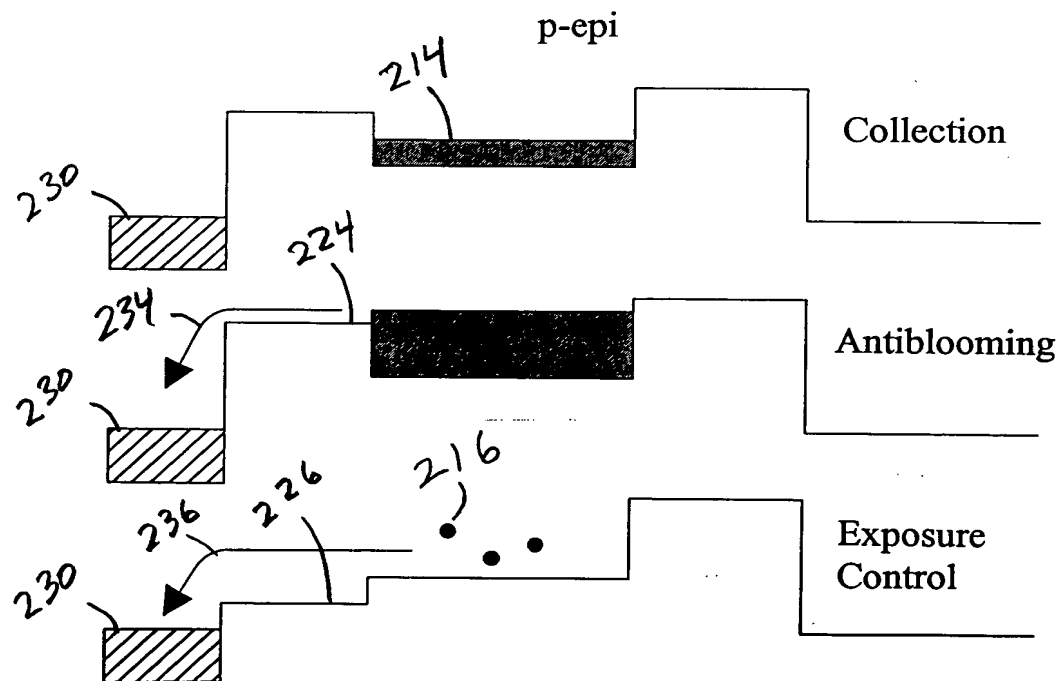
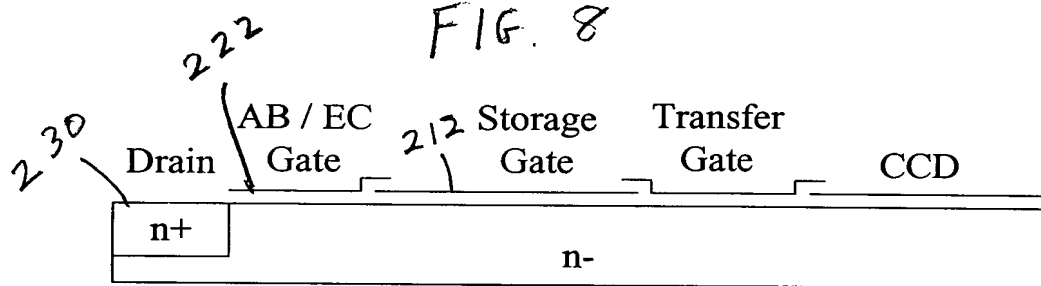


FIG. 9